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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/679,854	10/05/2000	Kathleen A. Duncan	9785980-0079	9183

25700 7590 04/08/2004

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
YE, LIN	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 04/08/2004

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/679,854	Applicant(s) DUNCAN ET AL.	
	Examiner Lin Ye	Art Unit 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33-40* is/are allowed.

6)☒ Claim(s) *1-32 and 41-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4, 6, 12*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 5 is objected to because of the following informalities:

For Claim 5 (line 3) recites the limitation "the programmable addresser". There is insufficient antecedent basis for this limitation in the claim. It should be changed to -- the programmable **input** addresser--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S. C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 4-32 and 41-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Duncan et al. U.S. Patent 6,597,394.

Referring to claim 1, the Duncan reference discloses in Figures 1-6, an image transform processor for processing image data, comprising: a programmable arithmetic processor (Arithmetic 450 as shown in Figure 4) capable of receipt of the image data from a data source (analog Signal processor 211 and A/D converter 212) over a data path and processing the digital image data; and a programmable input addresser (input addresser 430 included in

programmable addressing block 410) that controls transfer of the image data from the data source (211) to the programmable arithmetic processor by providing a source address onto a source address path, the source address identifying the data source (See Col. 6, lines 15-31).

Referring to claim 2, the Duncan reference discloses wherein the programmable input addresser (430) further controlling transfer of the image data to the programmable arithmetic processor by providing a storage address to the programmable arithmetic processor (450), the storage address identifying a location within the programmable arithmetic processor for storage of the digital image data as shown in Figure 4 (See Col. 8, lines 63-67 and Col. 9, lines 5-23).

Referring to claim 4, the Duncan reference discloses wherein the data source being a memory (DRAM), the source address being a memory address identifying a location of the image data within the memory (See Col. 5, lines 61-67 and Col. 6, lines 1-9).

Referring to claim 5, the Duncan reference discloses wherein the data source being a memory (DRAM), the source address path being a read address bus coupled between the programmable addresser (430) and the memory, the source address being a memory address identifying a location of the digital image data within the memory (See Col. 7, lines 12-25).

Referring to claim 6, the Duncan reference discloses wherein the storage location within the programmable arithmetic processor being a local buffer as shown in Figure 6A and 6C (shifting register 610, see Col. 15, lines 15-30).

Referring to claim 7, the Duncan reference discloses wherein storage location within the programmable arithmetic processor being a plurality of local buffer as shown in Figure 6A and 6C (pipeline registers 702-710, see Col. 15, lines 15-30).

Referring to claim 8, the Duncan reference discloses wherein a programmable output addresser controlling transfer of the image data from the programmable arithmetic processor to a memory by providing a write address onto a write path, the write address identifying a write address in the memory for storage of the digital image data (See Col. 14, lines 24-39).

Referring to claim 9, the Duncan reference discloses wherein the write path is a write address bus (address bus in Figure 5A) electrically connected to the programmable output addresser and the memory (DRAM) (See Col. 13, lines 47-52).

Referring to claim 10, the Duncan reference discloses wherein he programmable output addresser further controlling transfer of the image data by providing a retrieval address to the programmable arithmetic processor, the retrieval address identifying a location within the programmable arithmetic processor for retrieval of the image data (See Col. 14, lines 56-64).

Referring to claim 11, the Duncan reference discloses wherein the retrieval location within the programmable arithmetic processor is a buffer (accumulator 680, See Col. 15, lines 59-62)

Referring to claim 12, the Duncan reference discloses wherein the retrieval location within the programmable arithmetic processor is at least one buffer (680) of a plurality of buffers (accumulators 680, 682, 684, see Col. 15, lines 59-67).

Referring to claim 13, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claims 1, 4 and 6.

Referring to claim 14, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claims 1, 4, 6, 8 and 10.

~~Referring to claim 2, the Duncan reference discloses wherein~~

Referring to claim 15, the Duncan reference discloses in Figure 6A, wherein image transform processor having a plurality of buffers, a method comprising: providing a first portion of an input image in a first buffer of a plurality of buffers (latches 640-643); performing a first processing operation (by adder 644 and 645) on the first portion of the input image to define a first processed image data portion; storing the first processed image data portion in a second buffer of the plurality of buffers (latches 646 and 647): providing a second portion of the input image (Second image data input from input addresser holding latch to arithmetic block 450 repeatedly) in the first buffer (latches 640-643); and performing a second processing operation (by adder 648) on the first processed image data portion to define a second processed image data portion (See Col. 15, lines 46-63).

Referring to claim 16, the Duncan reference discloses wherein storing the second processed image data portion in a third buffer (output latch 650) of the plurality of buffers (See Col. 15, lines 46-63).

Referring to claim 17, the Duncan reference discloses wherein performing the first processing operation (by adder 644 and 645) on the second portion of the input image to define a third processed image data portion as shown in Figure 6A (See Col. 15, lines 46-63).

Referring to claim 18, the Duncan reference discloses wherein storing the third processed image data portion in the second buffer (latches 646 and 647).

Referring to claim 19, the Duncan reference discloses wherein providing the second processed image data portion onto a data path as output image data (output latch 650 outputs data to output addresser holding latch as shown in Figure 6A)

Referring to claim 20, the Duncan reference discloses wherein the second portion of the input image being provided in the first buffer (latches 640-643) concurrently with the second processing operation (by adder 648) being performed on the first processed image data portion (Microsequencer sequentially controls the data output from shifter Registrar 610 repeatedly).

Referring to claim 21, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 15, and providing, concurrently (the shift registers can be programmed and controls the image data processing by each steps through from the latches, see Col. 52-62) with the second processing operation being perform on the first processed image data portion, a second portion of the input image in the first buffer.

Referring to claim 22, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 15, and providing a second portion of the input image in a third buffer (latch 647) of the plurality of buffers; performing a second processing operation on the first processed image data portion to define second processed image data portion; and storing the second processed image data in a fourth one of the buffers (latch 650).

Referring to claim 23, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 17

Referring to claim 24, the Duncan reference discloses wherein storing the third processed image data portion in a fifth buffer (accumulator 680) of the plurality of buffers.

Referring to claim 25, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 21, and wherein the second portion of the input

image is provided in the third buffer concurrently with the second processing operation being performed on the first processed image data portion (Microsequencer sequentially controls the data output from shifter Registrar 610 repeatedly).

Referring to claim 26, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 15.

Referring to claim 27, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 16.

Referring to claim 28, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 17.

Referring to claim 29, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 18.

Referring to claim 30, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 19.

Referring to claim 31, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 21.

Referring to claim 32, the Duncan reference discloses wherein the processor is a single instruction multiple data (SIMD) processor (Microsequencer 602, See Col. 17, lines 1-5).

Referring to claim 41, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 22.

Referring to claim 42, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 23.

Referring to claim 43, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 24.

Referring to claim 44, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 1.

Referring to claim 45, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 8.

Referring to claim 46, the Duncan reference discloses all subject matter as discussed with respected to same comment as with claim 13.

4. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhang U.S. Patent 5,812, 195.

Referring to claim 1, the Zhang reference discloses in Figures 4 and 4B, an image transform processor (digital array processor section 420) for processing image data, comprising: a programmable arithmetic processor (signal processor 422) capable of receipt of the image data from a data source (image processor 431) over a data path (470) and processing the digital image data; and a programmable (program controller 424 controls the address generator 423 can be consider as programmable input addresser) input addresser that controls transfer of the image data from the data source (image processor 431) to the programmable arithmetic processor by providing a source address onto a source address path, the source address identifying the data source (See Col. 15, lines 56-65).

Referring to claim 3, the Zhang reference discloses wherein the data source being a frame capture processor (the input video from camera 101 is digitized and decoded by image

processor 431), the source address identifying the frame capture processor (See Col. 16, lines 10-15).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 3 is rejected under 35 U.S. C. 103(a) as being unpatentable over Duncan et al. U.S. Patent 6,597,394 in view of Hata et al. U.S Patent 6,100,928.

Referring to claim 3, the Duncan reference discloses all subject matter as discussed in respected claim 1, except the reference does not explicitly show wherein the data source being a frame capture processor, the source address identifying the frame capture processor. The Hata reference discloses in Figures 1 and 5, an image transform processor (Discrete Cosine Transforms 108) receipt of the image data from a frame capture processor (Image Pre-Processor 107) (See Col. 9, lines 40-52). The Hata reference is an evidence that one of ordinary skill in the art at the time to see more advantages for digital signal processing section including a Image pre-Processor to perform color correction, white balance and gamma functions before input data to the image transform processor so that a high quality

image can be recoding to recoding media. For that reason, it would have been obvious to see image transform processor receipts the data source being a frame capture processor, the source address identifying the frame capture processor disclosed by Duncan.

Allowable Subject Matter

7. Claims 33-40 allowed.

The following is an examiner's statement of reasons for allowance:

The prior art does not teach or fairly suggest an image transform processor comprising: a programmable input addresser to retrieve an image as a received image in accordance with a first programmed predefined access pattern, the programmable input addresser to output the received image in accordance with a second programmed predefined access pattern; a programmable output addresser; a SIMD processor including a controller coupled to a memory storing an at least one image processing instructions, the SIMD processor having a plurality of processing elements and a plurality of local buffers arranged in a plurality of levels and a plurality of processing banks, each processing bank in the plurality of processing banks being connected in parallel with another processing banks in the plurality of processing banks, the controller being coupled to each processing element in the plurality of processing elements and each local buffer in the plurality of local buffers to control the operation of each processing element and each local buffer such that the plurality of processing banks simultaneously respond to an instruction from the controller, the SIMD processor being arranged as: (i) a first level of the plurality of levels including a first set of local buffers from the plurality of local buffers; (ii) a second level of the plurality of levels

including a second set of local buffers from the plurality of local buffers; (iii) a third level of the plurality of levels including a third set of local buffers from the plurality of local buffers; (iv) a fourth level of the plurality of levels including a fourth set of local buffers from the plurality of local buffers; (v) a processing level including a set of processing elements from the plurality of processing elements that generates a processed image from the image stored in the plurality of local buffers in accordance with an image processing instruction; each processing bank including one local buffer of the first set of local buffers, one local buffer of the second set of local buffers, a processing element from the set of processing elements, one local buffer of the third set of local buffers, and one local buffer of the fourth set of local buffers, the processing element of each processing bank storing and retrieving the image in response to the image processing instruction; where the processing element associated with each processing bank directly read from and store to the local buffers of an adjacent processing bank, if any; each processing bank receiving an image from the programmable input addresser via the first set of local buffers, each processing bank also receiving the image from an input block addresser via the second set of local buffers, each processing bank outputting the processed image to the programmable output addresser via the third set of local buffers, each bank also sending the processed image to the programmable output addresser via the fourth set of local buffers; where the image processing instruction include an instruction that selectively designate one of the group consisting of the first level and the second level to receive the image from the programmable input block addresser as a selected input level, and a non-selected input level, such that simultaneously the selected input level receives the image while the processing element processes the image from the non-selected

input level; where the image processing instruction include an instruction that selectively designate one of the group consisting of the third level and the fourth level to output the processed image to an output block addresser as a selected output level, and a non-selected output level, such that simultaneously the selected output level sends the processed image data while the processing element processes the image from the non-selected output level; and the programmable output addresser to receive the processed image from the selected output level, the output block addresser to output the processed image in accordance with a programmed predefined output pattern.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lin Ye whose telephone number is (703) 305-3250. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R Garber can be reached on (703) 305-4929.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC. 20231

Or faxed to:

(703) 872-9306

Hand-delivered responses should be brought to Crystal Park 11, 2121 Crystal drive,

Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Lin Ye

March 29, 2004

NGOC YEN VU
PRIMARY EXAMINER